What is claimed is:

1. A split gate flash memory cell, comprising:

a substrate having a trench therein;

a conductive layer disposed on the bottom of the trench;

a pair of source regions, each disposed in the substrate adjacent to one sidewall of the trench and electrically connected by the conductive layer;

a source isolation layer disposed on the conductive layer;

a pair of tunnel oxide layers, respectively disposed on one sidewall of the trench and on the source isolation layer;

a U-shaped floating gate having a plurality of inside tips disposed on the source isolation layer and contacting the tunnel oxide layers thereby;

an inter-gate dielectric layer disposed on the U-shaped floating gate;

a control gate disposed on the inter-gate dielectric;

a conductive stud disposed on the control gate; and

a drain region disposed in the substrate adjacent to the trench.

2. The cell as claimed in claim 1, wherein a bottom insulating layer is further disposed under the conductive layer.

3. The cell as claimed in claim 2, wherein the bottom insulating layer is silicon dioxide.

4. The cell as claimed in claim 1, wherein the U-shaped floating gate and the control gate are N-type dopant doped polysilicon.

5. The cell as claimed in claim 1, wherein the inter-gate dielectric layer is silicon dioxide.

6. The cell as claimed in claim 1, wherein the conductive layer is N-type dopant doped polysilicon.

7. The cell as claimed in claim 1, wherein the tunnel oxide layer is silicon dioxide.

8. The cell as claimed in claim 1, wherein the conductive stud is N-type dopant doped polysilicon.

9. The cell as claimed in claim 1, wherein a connecting oxide layer is further disposed between the U-shaped control gate and the inter-gate dielectric layer.

10. The as claimed in claim 9, wherein the connecting oxide layer is silicon dioxide.

11. The as claimed in claim 1, wherein the substrate is P-type silicon substrate.

12. A method of fabricating split gate flash memory cells, comprising the steps of:

providing a substrate;

forming a plurality of parallel long trenches along a first direction in the substrate;

forming a conductive layer and a pair of source regions on the bottom of each long trench, wherein the source regions are respectively disposed in the substrate adjacent to two sidewalls of each long trench and electrically connected by the conductive layer therein;

forming a source isolation layer on each conductive layer;

forming a tunnel oxide on two sidewalls of each long trench;

forming a U-shaped floating gate with a plurality of inside tips and a connecting oxide layer therein on each source isolation layer;

forming an inter-gate dielectric layer on each U-shaped floating gate and the connecting oxide layer therein;

forming a control gate on each inter-gate dielectric layer;

forming a conductive stud on each control gate;

forming a plurality of parallel shallow trench isolation (STI) regions along a second direction, defining a plurality of cell trenches; and

forming a drain region in the substrate adjacent to each cell trench.

13. The method as claimed in claim 12, wherein the first direction is perpendicular to the second direction.

14. The method as claimed in claim 12, wherein the substrate is P-type silicon substrate.

15. The method as claimed in claim 12, further comprising before forming a plurality of parallel long trenches along a first direction in the substrate, the step of sequentially forming a pad oxide layer and a mask layer on the substrate.

16. The method as claimed in claim 15, wherein the mask layer is silicon nitride.

17. The method as claimed in claim 15, wherein the pad oxide layer is silicon dioxide.

18. The method as claimed in claim 12, further comprising before forming a conductive layer and a pair of source regions on the bottom of each long trench, the step of forming a bottom insulating layer on the bottom of each long trench.

19. The method as claimed in claim 12, wherein forming a conductive layer and a pair of source regions on the bottom of each long trench further comprises the steps of:

forming a source material layer in each long trench;

performing a high temperature annealing process, driving out dopants in the source material layer, forming a pair of source regions in the substrate adjacent to two sidewalls of each long trench, electrically connected by the conductive layer therebetween; and

removing the source material layer from each long trench.

20. The method as claimed in claim 19, wherein the source material layer is N-type doped silicon dioxide.

21. The method as claimed in claim 20, wherein the N-type doped silicon dioxide comprises phosphorous (P) doped silicon dioxide or arsenic (As) doped silicon dioxide.

22. The method as claimed in claim 12, further comprising before forming a tunnel oxide on two sidewalls of each long trench, performing a threshold voltage implantation on the sidewalls of each long trench.

23. The method as claimed in claim 12, wherein forming a U-shaped floating gate with a plurality of inside tips and a connecting oxide layer therein on the source isolation layer further comprises:

conformably depositing a floating gate layer in each long trench;

forming a connecting oxide layer on the floating gate layer in each long trench;

removing portions of the floating gate layer exposed by the connecting oxide layer, forming a U-shaped floating gate with the connecting oxide layer therein;

forming a floating gate oxide spacer on sidewalls of each long trench;

forming a floating gate nitride spacer on the floating gate oxide spacer;

partially etching the connecting oxide, exposing part of the inside U-shaped floating gate;

isotropically etching the inside U-shaped floating gate, forming a plurality of tips on the insides thereof; and

removing the floating gate oxide spacers, the floating gate nitride spacers, and part of the tunnel oxides adjacent to the sidewalls of each long trench, leaving a U-shaped floating gate with a plurality of inside tips and a connecting oxide layer therein.

24. The method as claimed in claim 23, wherein the method for partially etching the connecting oxide is wet etching.

25. The method as claimed in claim 12, further comprising before forming a conductive stud on the control gate, the step of forming control gate spacers on sidewalls of each long trench.

26. The method as claimed in claim 25, wherein the control gate spacer is silicon dioxide.

27. The method as claimed in claim 12, wherein forming a plurality of parallel shallow trench isolation (STI) regions along a second direction, and defining a plurality of cell trenches further comprises:

sequentially performing a photolithography process and an etching process, defining a plurality of parallel long isolation trenches along a second direction, stopping at the source isolation layer therein; and

forming an insulating layer in the long isolation trenches.

28. The method as claimed in claim 27, wherein the insulating layer is silicon dioxide.

29. The method as claimed in claim 27, wherein the method of forming the insulating layer is high density plasma enhanced chemically vaporization deposition (HDP CVD).

30. The method as claimed in claim 12, wherein forming a drain region in the substrate adjacent to each of the cell trenches further comprises:

removing the mask layer, exposing the pad oxide layer;

performing a drain implantation;

performing a thermal annealing process, forming a drain region in the substrate adjacent to each cell trenches;

removing the pad oxide layer; and

forming a second insulating layer on each drain region.

31. The method as claimed in claim 30, wherein impurities used in the drain region implantation are N-type impurities.

32. The method as claimed in claim 31, wherein the N-type impurities are phosphorous (P) ions or arsenic (As) ions.